IN THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the Application:

LISTING OF CLAIMS:

1. (Original) In a memory circuit board that stores a cache for a data storage system, a method comprising the steps of:

receiving a communication that includes a script command and a payload, the payload including a series of individual instructions;

in response to the script command, parsing the payload to identify the series of individual instructions; and

performing a series of operations in accordance with the identified series of individual instructions.

2. (Original) The method of claim 1 wherein the cache includes memory locations which store a data element, wherein an individual instruction of the series of individual instructions includes an address referencing the memory locations which store the data element, and wherein the step of performing the series of operations includes the steps of:

selecting the data element based on the address of the individual instruction;

retrieving the data element from the memory locations of the cache; and

performing an operation based on the individual instruction, the operation using the data element as at least one parameter of the operation.

3. (Original) The method of claim 1 wherein the memory circuit board further stores an instruction library, wherein the series of individual instructions includes an instruction reference that points to a section of code of the instruction library, and wherein the step of performing the series of operations includes the steps of:

referencing the section of the code of the instruction library based on the instruction reference; and

executing the section of code.

4. (Original) The method of claim 1 wherein the steps of parsing and performing occur as an atomic operation.

5. (Original) The method of claim 1, further comprising the step of:

generating a series of results in response to performing the series of operations; and

providing the series of results to a processor circuit board.

6. (Original) The method of claim 5 wherein the step of providing the series of results to the processor circuit board includes the steps of:

packaging the series of results in a set of data blocks; and

transferring the set of data blocks to the processor circuit board.

7. (Original) The method of claim 1, further comprising the step of:

loading a set of parameters into a set of registers of the memory circuit board to enable the set of parameters to be used when performing the series of operations.

8. (Original) A data storage system, comprising:

(a) a set of storage devices;

(b) a memory circuit board that stores a cache to temporarily store copies of data elements stored in the set of storage devices; and

(c) a processor circuit board that operates as at least one of a front-end interface between an external device and the cache and a back-end interface between the cache and the set of storage devices, wherein the memory circuit board is configured to:

(i) receive, from the processor circuit board, a communication that includes a script command and a payload, the payload including a series of individual instructions,

(ii) parse the payload to identify the series of individual instructions in response to the script command, and

(iii) perform a series of operations in accordance with the identified series of individual instructions.

9. (Original) The data storage system of claim 8 wherein the cache includes memory locations which store a data element, wherein an individual instruction of the series of individual instructions includes an address referencing the memory locations which store the data element, and wherein the memory circuit board is configured to perform at least a portion of the series of operations by:

selecting the data element based on the address of the individual instruction;

retrieving the data element from the memory locations of the cache; and

performing an operation based on the individual instruction, the operation using the data element as at least one parameter of the operation.

10. (Original) The data storage system of claim 8 wherein the memory circuit board further stores an instruction library, wherein the series of individual instructions includes an instruction reference that points to a section of code of the instruction library, and wherein the memory circuit board is configured to perform at least a portion of the series of operations by:

referencing the section of the code of the instruction library based on the instruction reference; and

executing the section of code.

11. (Original) The data storage system of claim 8 wherein the memory circuit board is configured to receive the communication, parse the payload, and perform the series of operations as an atomic operation.

12. (Original) The data storage system of claim 8 wherein the memory circuit board is further configured to:

generate a series of results in response to performing the series of operations; and

provide the series of results to the processor circuit board.

13. (Original) The data storage system of claim 12 wherein the memory circuit board is configured to provide the series of results by:

packaging the series of results in a set of data blocks; and

transferring the set of data blocks to the processor circuit board.

14. (Original) The data storage system of claim 8 wherein the memory circuit board is further configured to:

load a set of parameters into a set of registers of the memory circuit board to enable the set of parameters to be used when performing the series of operations.

15. (Previously Presented) A memory circuit board for a data storage system, comprising:

(a) an input/output port to connect with a processor circuit board of the data storage system;

(b) a set of memory locations, at least some of the memory locations forming a cache that temporarily stores copies of data elements stored in a set of storage devices of the data storage system; and

(c) a controller coupled to the input/output port and the set of memory locations, wherein the controller is configured to:

(i) receive, from the processor circuit board through the input/output port, a communication that includes a script command and a payload, the payload including a series of individual instructions,

(ii) parse the payload to identify the series of individual instructions in response to the script command, and

(iii) perform a series of operations in accordance with the identified series of individual instructions.

16. (Original) The memory circuit board of claim 15 wherein the cache includes memory locations which store a data element, wherein an individual instruction of the series of individual instructions includes an address referencing the memory locations which store the data element, and wherein the controller is configured to perform at least a portion of the series of operations by:

selecting the data element based on the address of the individual instruction;

retrieve the data element from the memory locations of the cache; and

perform an operation based on the individual instruction, the operation using the data element as at least one parameter of the operation.

17. (Previously Presented) The memory circuit board of claim 15 wherein the set of memory locations holds an instruction library, wherein the series of individual instructions includes an instruction reference that points to a section of code of the instruction library, and wherein the controller is configured to perform at least a portion of the series of operations by:

referencing the section of the code of the instruction library based on the instruction reference; and

executing the section of code.

18. (Original) The memory circuit board of claim 15 wherein the memory circuit board is configured to receive the communication, parse the payload, and perform the series of operations as an atomic operation.

19. (Original) The memory circuit board of claim 15 wherein the controller is further configured to:

generate a series of results in response to performing the series of operations; and

provide the series of results to the processor circuit board.

20. (Original) The memory circuit board of claim 19 wherein the controller is configured to provide the series of results by:

packaging the series of results in a set of data blocks; and

transferring the set of data blocks to the processor circuit board.

21. (Original) The memory circuit board of claim 15 wherein the controller is further configured to:

load a set of parameters into a set of registers of the memory circuit board to enable the set of parameters to be used when performing the series of operations.

22. (Original) A processor circuit board for a data storage system, comprising:

(a) an input/output port to connect with a memory circuit board of the data storage system; and

(b) control circuitry coupled to the input/output port, wherein the control circuitry is configured to provide, to the memory circuit board through the input/output port, a communication that includes a script command and a payload, wherein the payload includes a series of individual instructions, and wherein the script command is configured to direct the memory circuit board to:

(i) parse the payload to identify the series of individual instructions in response to the script command, and

(ii) perform a series of operations in accordance with the identified series of individual instructions.

23. (Previously Presented) The method of claim 1 wherein the series of individual instructions of the payload has a positional order, and wherein the step of performing the series of operations includes the step of:

processing the series of individual instructions in the positional order within the memory circuit board to effectuate temporary caching of data within the memory circuit board, the data being en route between an external host and a set of disk drives of the data storage system.

24. (Previously Presented) The method of claim 23 wherein the step of receiving the communication includes the step of:

acquiring the communication including the script command and the payload, which has the series of individual instructions, from a processor circuit board through a multi-drop bus which is configured to carry communications between multiple processor circuit boards and multiple memory circuit boards of the data storage system, the processor circuit board being configured to exert control over the memory circuit board using the script command and payload.

25. (Previously Presented) The data storage system of claim 8 wherein the series of individual instructions of the payload has a positional order, and wherein the memory circuit board, when performing the series of operations, is configured to:

process the series of individual instructions in the positional order within the memory circuit board to effectuate temporary caching of data within the memory circuit board, the data being en route between an external host and a set of disk drives of the data storage system.

26. (Previously Presented) The data storage system of claim 25 wherein the memory circuit board, when receiving the communication, is configured to:

acquire the communication including the script command and the payload, which has the series of individual instructions, from the processor circuit board through a multi-drop bus which is configured to carry communications between multiple processor circuit boards and multiple memory circuit boards of the data storage system, the processor circuit board being configured to exert control over the memory circuit board using the script command and payload.

27. (Previously Presented) The memory circuit board of claim 15 wherein the series of individual instructions of the payload has a positional order, and wherein the controller, when performing the series of operations, is configured to:

process the series of individual instructions in the positional order within the memory circuit board to effectuate temporary caching of data within the memory circuit board , the data being en route between an external host and a set of disk drives of the data storage system.

28. (Previously Presented) The memory circuit board of claim 27 wherein the controller, when receiving the communication, is configured to:

acquire the communication including the script command and the payload, which has the series of individual instructions, from the processor circuit board through a multi-drop bus which is configured to carry communications between multiple processor circuit boards and multiple memory circuit boards of the data storage system, the processor circuit board being configured to exert control over the memory circuit board using the script command and payload.

29. (Previously Presented) The processor circuit board of claim 22 wherein the series of individual instructions of the payload has a positional order, and wherein the control circuitry, providing the communication, is configured to:

output the series of individual instructions in the positional order to the memory circuit board to effectuate temporary caching of data within the memory circuit board, the data being en route between an external host and a set of disk drives of the data storage system.

30. (Previously Presented) The processor circuit board of claim 29 wherein the control circuitry, when outputting the communication, is configured to:

send the communication including the script command and the payload, which has the series of individual instructions, from the processor circuit board through a multi-drop bus which is configured to carry communications between multiple processor circuit boards and multiple memory circuit boards of the data storage system, the control circuitry being configured to exert control over the memory circuit board using the script command and payload.